RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

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August 29, 2008 — Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/006,785	Confirmation No.	: 1320
Applicant	: Todd A. Merritt		
Filed	: November 9, 2001	Attorney Docket No.:	500345.02 (29616/US/1)
Art Unit	: 2185	Customer No.	: 27,076
Examiner	: Denise Tran		
Title	: OUTPUT BUFFER HAVING INHERENTLY PRECISE DATA MASKING		

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RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicant acknowledges receipt of the Office Action dated August 11, 2008.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 45, and 52, as follows:

1. (Twice Amended) An output buffer[s], comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and

second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values.

45. (Amended) The output buffer of claim [43] 40 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased enable and data input signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased enable signal and a respective differently-phased data input signal, the latches being selectively coupled to the data input terminals responsive to their respective

data input signals and being coupled to the data output terminal responsive to their respective enable signals, the data input signals being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data output terminals after being stored in each of the latches for a predetermined period.

52. (Amended) The dynamic random access memory of claim [50] 47 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased input data enable signals and output data enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased input data enable signal and a respective differently-phased output data enable signal, the latches being selectively coupled to the data input terminals responsive to their respective input data enable signals and being coupled to the data read output terminals responsive to their respective output data enable signals, the output data signals from the data ports of the array being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data read output terminals after being stored in each of the latches for a predetermined period.